



Shri Vaishnav Vidyapeeth Vishwavidyalaya, Indore

Shri Vaishnav Institute of Technology and Science

Choice Based Credit System (CBCS) in the Light of NEP-2020

Diploma in Mechatronics Engineering

( Common to EI/MX/ET)

(2021-2024)

COURSE CODE	CATEGORY	COURSE NAME	TEACHING & EVALUATION SCHEME								
			THEORY			PRACTICAL		L	T	P	CREDITS
			END SEM University Exam	Two Term Exam	Teachers Assessment*	END SEM University Exam	Teachers Assessment*				
DTEI301	DCC	MEASUREMENT AND INSTRUMENTATION	60	20	20	30	20	2	1	2	4

**Legends:** L - Lecture; T - Tutorial/Teacher Guided Student Activity; P – Practical; C - Credit;

\***Teacher Assessment** shall be based following components: Quiz/Assignment/ Project/Participation in Class, given that no component shall exceed more than 10 marks.

#### Course Educational Objectives (CEOs):

1. To introduce the basic functional elements of instrumentation.
2. To introduce the fundamentals of electrical and electronic instruments.
3. To educate on the comparison between various measurement techniques.
4. To introduce various storage and display devices.
5. To introduce various transducers and the data acquisition system.

#### Course Outcomes (COs):

After completion of this course the students are expected to be able to demonstrate following knowledge, skills, and attitudes.

The students will be able to

1. To apply knowledge of measurement system.
2. To identify, formulate, and solve the fundamentals of electrical and electronic instruments.
3. Demonstrate various types of introduce various modern storage and display devices.
4. Demonstrate various types of transducers and the data acquisition system.

#### Syllabus

##### UNIT I

8Hrs.

**Introduction to measurement:** Definition, application and types of measurement System, Accuracy, Precision, sensitivity, Resolution. Functional elements of an instrument, Static and dynamic characteristics, Errors in measurement, Statistical evaluation of measurement data, Standards and calibration.

Chairperson  
Board of Studies  
Shri Vaishnav Vidyapeeth  
Vishwavidyalaya, Indore

Chairperson  
Faculty of Studies  
Shri Vaishnav Vidyapeeth  
Vishwavidyalaya Indore

Controller of Examinations  
Shri Vaishnav Vidyapeeth  
Vishwavidyalaya Indore

Joint Registrar  
Shri Vaishnav Vidyapeeth  
Vishwavidyalaya Indore



**Shri Vaishnav Vidyapeeth Vishwavidyalaya, Indore**  
**Shri Vaishnav Institute of Technology and Science**  
**Choice Based Credit System (CBCS) in the Light of NEP-2020**  
**Diploma in Mechatronics Engineering**  
**( Common to EI/MX/ET)**  
**(2021-2024)**

COURSE CODE	CATEGORY	COURSE NAME	TEACHING & EVALUATION SCHEME								
			THEORY			PRACTICAL		L	T	P	CREDITS
			END SEM University Exam	Two Term Exam	Teachers Assessment*	END SEM University Exam	Teachers Assessment*				
DTEI301	DCC	MEASUREMENT AND INSTRUMENTATION	60	20	20	30	20	2	1	2	4

**Legends:** L - Lecture; T - Tutorial/Teacher Guided Student Activity; P – Practical; C - Credit;  
\*Teacher Assessment shall be based following components: Quiz/Assignment/ Project/Participation in Class, given that no component shall exceed more than 10 marks.

**UNIT II**

**9Hrs.**

**Electrical and Electronics Instruments:**

Construction and operation of moving coil, moving iron, Theory and Operation of D'Arsonval. Principle and types of analog and digital voltmeters, ammeters, Determination of B-H curve and measurements of iron loss, Instrument transformers, Instruments for measurement of frequency and phase.

**UNIT III**

**7Hrs.**

**Comparison Methods of Measurements**

D.C & A.C potentiometers, D.C & A.C bridges, transformer ratio bridges, self-balancing bridges. Interference & screening, Multiple earth and earth loops, Electrostatic and electromagnetic interference, Grounding techniques.

**UNIT IV**

**6Hrs.**

**Modern Storage and Display Devices**

Compact Disk CD), DVDs, USB Flash Drive, Hard Drive/SSD, Cloud Storage, OLED, Micro-LED display, Nano-cell Technology, Quantum dot LED (QLED).

**UNIT V**

**7Hrs.**

**Transducers and Data Acquisition Systems**

Classification of transducers based upon Transduction principle, Introduction to Smart sensors and Micro Sensors, Introduction to Data Acquisition System (DAS) and its Industrial Application.

**Chairperson**  
Board of Studies  
Shri Vaishnav Vidyapeeth  
Vishwavidyalaya, Indore

**Chairperson**  
Faculty of Studies  
Shri Vaishnav Vidyapeeth  
Vishwavidyalaya Indore

**Controller of Examinations**  
Shri Vaishnav Vidyapeeth  
Vishwavidyalaya Indore

**Joint Registrar**  
Shri Vaishnav Vidyapeeth  
Vishwavidyalaya Indore





**Shri Vaishnav Vidyapeeth Vishwavidyalaya, Indore**  
**Shri Vaishnav Institute of Technology and Science**  
**Choice Based Credit System (CBCS) in the Light of NEP-2020**  
**Diploma in Mechatronics Engineering**  
**( Common to EI/MX/ET)**  
**(2021-2024)**

COURSE CODE	CATEGORY	COURSE NAME	TEACHING & EVALUATION SCHEME								
			THEORY			PRACTICAL		L	T	P	CREDITS
			END SEM University Exam	Two Term Exam	Teachers Assessment*	END SEM University Exam	Teachers Assessment*				
DTEI301	DCC	MEASUREMENT AND INSTRUMENTATION	60	20	20	30	20	2	1	2	4

**Legends:** L - Lecture; T - Tutorial/Teacher Guided Student Activity; P – Practical; C - Credit;  
**\*Teacher Assessment** shall be based following components: Quiz/Assignment/ Project/Participation in Class, given that no component shall exceed more than 10 marks.

**Text Books:**


1. H.S. Kalsi, "Electronic Instrumentation", Tata McGraw Hill, 4th Edition 2019.
2. D.V.S. Moorthy, "Transducers and Instrumentation", Prentice Hall of India Pvt Ltd, 2<sup>nd</sup> Edition 2011.


**References:**

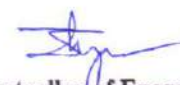
1. A.J. Bouwens, "Digital Instrumentation", Tata McGraw Hill, 1997.
2. Martin Reissland, "Electrical Measurements", New Age International (P) Ltd., Delhi, 2001.

**List of Experiments:**

1. Study of CRO and perform component testing using CRO.
2. Study of phase & frequency using Lissajous pattern with help of CRO.
3. Study and Perform Strain using strain gauge.
4. To study and perform LVDT (Linear Variable Differential Transformer) characteristics.
5. Study of function generator with its application.
6. To study and observe the balance condition for the Maxwell's bridge.
7. To study and observe the balance condition for the Schering bridge.
8. To study and observe the balance condition for the Hay's Bridge.
9. To study and observe the balance condition for the Wein's bridge.
10. To study and observe the balance condition for the Anderson's Bridge.

  
**Chairperson**  
Board of Studies  
Shri Vaishnav Vidyapeeth  
Vishwavidyalaya Indore

  
**Chairperson**  
Faculty of Studies  
Shri Vaishnav Vidyapeeth  
Vishwavidyalaya Indore

  
**Controller of Examinations**  
Shri Vaishnav Vidyapeeth  
Vishwavidyalaya Indore

  
**Joint Registrar**  
Shri Vaishnav Vidyapeeth  
Vishwavidyalaya Indore



**Shri Vaishnav Vidyapeeth Vishwavidyalaya, Indore**  
**Shri Vaishnav Institute of Technology and Science**  
**Choice Based Credit System (CBCS) in the Light of NEP-2020**  
**Diploma in Mechatronics Engineering**  
**(Common to MX/ET)**  
**(2021-2024)**

COURSE CODE	CATEGORY	COURSE NAME	TEACHING & EVALUATION SCHEME								
			THEORY			PRACTICAL		L	T	P	CREDITS
			END SEM University Exam	Two Term Exam	Teachers Assessment*	END SEM University Exam	Teachers Assessment*				
DTMT302	DCC	Basic Digital Electronics	60	20	20	30	20	3	0	2	4

**Legends:** L - Lecture; T - Tutorial/Teacher Guided Student Activity; P – Practical; C - Credit;  
\***Teacher Assessment** shall be based following components: Quiz/Assignment/ Project/Participation in Class, given that no component shall exceed more than 10 marks.

**Course Educational Objectives (CEOs):**

1. To present the Digital fundamentals, Boolean algebra, and its applications in digital systems
2. To present a problem oriented introductory knowledge of combinational digital circuits and its applications.
3. To explain the various semiconductor memories and related technology.
4. To introduce the sequential circuits involved in the making various digital circuits.

**Course Outcomes (COs):**

After completion of this course the students are expected to be able to demonstrate following knowledge, skills, and attitudes.

The students will be able to:

1. Describe the number systems, conversions, and their applications.
2. Apply minimization techniques such as K maps, Tabular method etc. for the design of digital circuits.
3. Understand combinational and sequential circuits.
4. Differentiate various type of memories and there use in different applications.

**Syllabus**

**UNIT I**

**10 Hrs.**

**Binary Number System:**

Binary arithmetic: addition, subtraction, multiplication and division, Complements: 1's, 2's, 9's

Chairperson  
Board of Studies  
Shri Vaishnav Vidyapeeth  
Vishwavidyalaya, Indore

Chairperson  
Faculty of Studies  
Shri Vaishnav Vidyapeeth  
Vishwavidyalaya, Indore

Controller of Examinations  
Shri Vaishnav Vidyapeeth  
Vishwavidyalaya, Indore

Joint Registrar  
Shri Vaishnav Vidyapeeth  
Vishwavidyalaya, Indore





**Shri Vaishnav Vidyapeeth Vishwavidyalaya, Indore**  
**Shri Vaishnav Institute of Technology and Science**  
**Choice Based Credit System (CBCS) in the Light of NEP-2020**  
**Diploma in Mechatronics Engineering**  
**(Common to MX/ET)**  
**(2021-2024)**

COURSE CODE	CATEGORY	COURSE NAME	TEACHING & EVALUATION SCHEME									
			THEORY			PRACTICAL			L	T	P	CREDITS
			END SEM University Exam	Two Term Exam	Teachers Assessment*	END SEM University Exam	Teachers Assessment*					
DTMT302	DCC	Basic Digital Electronics	60	20	20	30	20	3	0	2	4	

**Legends:** L - Lecture; T - Tutorial/Teacher Guided Student Activity; P – Practical; C - Credit;  
**\*Teacher Assessment** shall be based following components: Quiz/Assignment/ Project/Participation in Class, given that no component shall exceed more than 10 marks.

and 10's. Subtraction using complements, Octal number system, Hexadecimal number system, Conversion among binary, octal, decimal, and hexadecimal number systems, Codes: BCD, Gray, Excess-3, the parity bit.

**UNIT II**

**9Hrs.**

**Logic Gates and Boolean Algebra:**

Primary Gates: symbol, operation and truth-table, NAND, NOR, EX-OR, EX-NOR gates: symbol, operation, truth- table, Positive and Negative logic, De Morgan's theorems, Universal Gate, Laws and theorems of Boolean algebra, simplification of Boolean expression, Sum of products (SOP) and product of sums (POS) expression, Karnaugh maps: Four variable K-maps and their simplification techniques, Don't care condition.

**UNIT III**

**8Hrs.**

**Combinational Logic Circuits:**

Arithmetic Circuits: Half adder, full adder, parallel binary adder, 1's complement subtractor circuit, 2's complement subtractor/adder circuits, 8421 adder, half and full subtractor, parallel binary subtractor, Binary to gray and gray to binary code converters, Decoder and Encoder, Multiplexer and Demultiplexers.

**Chairperson**  
Board of Studies  
Shri Vaishnav Vidyapeeth  
Vishwavidyalaya, Indore

**Chairperson**  
Faculty of Studies  
Shri Vaishnav Vidyapeeth  
Vishwavidyalaya, Indore

**Controller of Examinations**  
Shri Vaishnav Vidyapeeth  
Vishwavidyalaya, Indore

**Joint Registrar**  
Shri Vaishnav Vidyapeeth  
Vishwavidyalaya, Indore



**Shri Vaishnav Vidyapeeth Vishwavidyalaya, Indore**  
**Shri Vaishnav Institute of Technology and Science**  
**Choice Based Credit System (CBCS) in the Light of NEP-2020**  
**Diploma in Mechatronics Engineering**  
**(Common to MX/ET)**  
**(2021-2024)**

COURSE CODE	CATEGORY	COURSE NAME	TEACHING & EVALUATION SCHEME								
			THEORY			PRACTICAL		L	T	P	CREDITS
			END SEM University Exam	Two Term Exam	Teachers Assessment*	END SEM University Exam	Teachers Assessment*				
DTMT302	DCC	Basic Digital Electronics	60	20	20	30	20	3	0	2	4

**Legends:** L - Lecture; T - Tutorial/Teacher Guided Student Activity; P – Practical; C - Credit;  
\***Teacher Assessment** shall be based following components: Quiz/Assignment/ Project/Participation in Class, given that no component shall exceed more than 10 marks.

#### UNIT IV

7Hrs.

##### Memory and Programmable Logic:

Memory Classifications, RAM: Static and Dynamic, ROM: ROM, PROM, EPROM.

Programmable Logic Array (PLA), Programmable Array Logic (PAL) and Structure. A/D and D/A Converter.

#### UNIT V

8Hrs.

##### Flip-Flops:

S-R latch, S-R flip-flops asynchronous and synchronous, timing diagram, truth table, excitation table, D flip floptiming diagram, truth table, excitation table T flip floptiming diagram, truth table, excitation table, J K flip flop timing diagram, truth table.

##### Text Books:

1. Mano M. M. and Ciletti M., "Digital Design", Pearson Education (2008) 4th ed.
2. Leach D. P., Malvino A. P., Saha G., "Digital Principles and Applications", TMH, (2014), 8th ed.

##### References:

1. Floyd T. L. and Jain R. P., "Digital Fundamentals", Pearson Education (2008) 10th ed.
2. Tocci R. and Widmer N., "Digital Systems: Principles and Applications", Pearson Education (2007) 10th ed.

Chairperson  
Board of Studies  
Shri Vaishnav Vidyapeeth  
Vishwavidyalaya, Indore

Chairperson  
Faculty of Studies  
Shri Vaishnav Vidyapeeth  
Vishwavidyalaya, Indore

Controller of Examinations  
Shri Vaishnav Vidyapeeth  
Vishwavidyalaya, Indore

Joint Registrar  
Shri Vaishnav Vidyapeeth  
Vishwavidyalaya, Indore





**Shri Vaishnav Vidyapeeth Vishwavidyalaya, Indore**  
**Shri Vaishnav Institute of Technology and Science**  
**Choice Based Credit System (CBCS) in the Light of NEP-2020**  
**Diploma in Mechatronics Engineering**  
**(Common to MX/ET)**  
**(2021-2024)**

COURSE CODE	CATEG ORY	COURSE NAME	TEACHING & EVALUATION SCHEME								
			THEORY			PRACTICAL		L	T	P	CREDITS
			END SEM University Exam	Two Term Exam	Teachers Assessment*	END SEM University Exam	Teachers Assessment*				
DTMT302	DCC	Basic Digital Electronics	60	20	20	30	20	3	0	2	4

**Legends:** L - Lecture; T - Tutorial/Teacher Guided Student Activity; P – Practical; C - Credit;

\***Teacher Assessment** shall be based following components: Quiz/Assignment/ Project/Participation in Class, given that no component shall exceed more than 10 marks.

**List of Experiments:**

1. To realize the basic logic gates.
2. To realize the NAND gate as a universal building block.
3. To realize the NOR gate as a universal building block.
4. To realize the HALF ADDER circuit
5. To realize the FULL ADDER circuit.
6. To realize the HALF SUBTRACTOR circuit.
7. To realize the AND-OR-INVERT circuit.
8. To realize the parity checker circuit.
9. To realize the exclusive-OR gate.
10. To realize the SR & JK flip-flop.

Chairperson  
Board of Studies  
Shri Vaishnav Vidyapeeth  
Vishwavidyalaya, Indore

Chairperson  
Faculty of Studies  
Shri Vaishnav Vidyapeeth  
Vishwavidyalaya, Indore

Controller of Examinations  
Shri Vaishnav Vidyapeeth  
Vishwavidyalaya, Indore

Joint Registrar  
Shri Vaishnav Vidyapeeth  
Vishwavidyalaya, Indore



**Shri Vaishnav Vidyapeeth Vishwavidyalaya, Indore**  
**Shri Vaishnav Institute of Technology and Science**  
**Choice Based Credit System (CBCS) in Light of NEP-2020**  
**Diploma in Electronics and Instrumentation Engineering**  
**(2022-2025)**

COURSE CODE	CATE-GORY	COURSE NAME	TEACHING & EVALUATION SCHEME								
			THEORY			PRACTICAL		L	T	P	CREDITS
			END SEM University Exam	Two Term Exam	Teachers Assessment*	END SEM University Exam	Teachers Assessment*				
DTEI307	DCC	Network Analysis	60	20	20	0	0	3	0	0	3

**Legends:** L - Lecture; T - Tutorial/Teacher Guided Student Activity; P – Practical; C - Credit;

\***Teacher Assessment** shall be based following components: Quiz/Assignment/ Project/Participation in Class, given that no component shall exceed more than 10 marks.

**Course Educational Objectives (CEOs):**

The subject aims to provide the student with:

1. An understanding of basic Network Circuits.
2. familiarization with various theorem.
3. Knowledge of various Two port networks.

**Course Outcomes (COs):**

Students will be able to:

1. Define network circuits.
2. Solve various theorem.
3. Solve Two port networks.

**Syllabus**

**UNIT I**

**8 Hrs.**

Preliminaries of Electrical elements R, L, C, and circuits; Ohm' Law , Kirchoff's laws Basic elements: Voltage and current sources, M; Linearity of elements, Elements in series and parallel Controlled sources.

**UNIT II**

**9 Hrs.**

Source transformations – Star Delta conversion, Power and energy in electrical elements. Circuit Analysis Methods: Nodal analysis, Mesh analysis. Theorems: Thevenin's, Norton , Max Power Transfer.

**UNIT III**

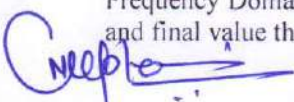
**8 Hrs.**

Transient Analysis: Source free RL and RC circuits, Elementary function unit step, unit ramp, unit impulse function and synthesis from source free parallel and series RLC circuit.

**UNIT IV**

**8 Hrs.**

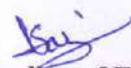
Frequency Domain Analysis: The phasor concept, sinusoidal steady state analysis; Laplace transform, initial and final value theorem. circuit analysis in s-domain.

  
**Chairperson**


Board of Studies  
Shri Vaishnav Vidyapeeth  
Vishwavidyalaya, Indore

  
**Chairperson**

Faculty of Studies  
Shri Vaishnav Vidyapeeth  
Vishwavidyalaya, Indore

  
**Controller of Examination**

Shri Vaishnav Vidyapeeth  
Vishwavidyalaya, Indore

  
**Joint Registrar**

Shri Vaishnav Vidyapeeth  
Vishwavidyalaya, Indore





**Shri Vaishnav Vidyapeeth Vishwavidyalaya, Indore**  
**Shri Vaishnav Institute of Technology and Science**  
**Choice Based Credit System (CBCS) in Light of NEP-2020**  
**Diploma in Electronics and Instrumentation Engineering**  
**(2022-2025)**

COURSE CODE	CATE-GORY	COURSE NAME	TEACHING & EVALUATION SCHEME								
			THEORY			PRACTICAL		L	T	P	CREDITS
			END SEM University Exam	Two Term Exam	Teachers Assessment*	END SEM University Exam	Teachers Assessment*				
DTEI307	DCC	Network Analysis	60	20	20	0	0	3	0	0	3

Legends: L - Lecture; T - Tutorial/Teacher Guided Student Activity; P - Practical; C - Credit;

\*Teacher Assessment shall be based following components: Quiz/Assignment/ Project/Participation in Class, given that no component shall exceed more than 10 marks.

**UNIT V**

**9 Hrs.**

Two Port Networks: Z, Y, h and ABCD parameters.

**Text Books:**

1.M.E. Van Valkenburg," Network Analysis", (Pearson), 2019.

**References:**

1.S P Ghosh A K Chakraborty," Network Analysis & Synth", (MGH).

2. Abhijit Chakrabarti, " Circuit Theory Analysis and Synthesis", Dhanpat Rai & Co. , 2018.

**Chairperson**

Board of Studies  
Shri Vaishnav Vidyapeeth  
Vishwavidyalaya, Indore

**Chairperson**

Faculty of Studies  
Shri Vaishnav Vidyapeeth  
Vishwavidyalaya, Indore

**Controller of Examination**

Shri Vaishnav Vidyapeeth  
Vishwavidyalaya, Indore

**Joint Registrar**

Shri Vaishnav Vidyapeeth  
Vishwavidyalaya, Indore